REMARKS

Claims 1-21 are pending in the current application. Claims 1 and 13 are independent claims. Claims 1-3, 5-8, 13-15, 17, 19 and 20 are amended. Amendments to the claims were made to correct minor typographical errors or overcome §112, second paragraph, problems noted in the Advisory Action. With regard to the amendment made to claims 1 and 13 with respect to claims 7 and 19, Applicants did not intend to imply that the exact subject matters of these dependent claims were incorporated into their respective independent claims. The Examiner will note that dependent claims 7 and 19 are different than the subject matters added into independent claims 1 and 13. No new matter has been added. In view of the following claims amendment and remarks, favorable reconsideration and allowance of the present application is respectfully requested.

In the Advisory Action dated December 19, 2006, the Examiner alleges that the term "cycle count" is being read too narrowly by Applicants. The Examiner further alleges that the present specification fails to "explicitly and deliberately" define "cycle count." Applicants disagree.

First, as remarked in Applicants amendment filed on November 27, 2006, a person of ordinary skill knows that a "cycle count" refers to cycle count values of a system clock, which means that cycle counts are dynamic. The '159 reference specifically teaches that **constant** C_n "represents the apparent value of each fetching scheme in reference to each other." Accordingly, **constant** C_n is not the same thing as cycle counts.

In addition, paragraph [0024] of the present application discloses:

> [0024] The demultiplexing controller 111 receives the decoder information for each decoded instruction. From the decoder information, the demultiplexing

> controller 111 determines the thread to which the decoded instruction belongs (e.g., from the operation type, from an instruction identifier, etc.). For each thread, the demultiplexing controller 111 assigns one of the cycle counters 113. When first assigned, the cycle counter 113 is reset or cleared to zero. When decoder information is received for an instruction of a thread, the demultiplexing controller 111 increments the cycle counter 113 associated with the thread by an amount corresponding to the number of cycle counts for processing the decoded instruction. Cycle counts refer to cycle count values of system clocks used by at least one of the instruction decoder 130, the register renamer 140, and the instruction queue unit 150, as non-limiting examples in processing the instruction. As explained previously, different operation types require different cycle counts of time to process. For example, a multiplication operation takes more cycle counts to process than an addition operation. Accordingly, the demultiplexing controller 111 uses the operation type of the decoded instruction to determine the number by which to increment the cycle counter. Stated another way, the demultiplexing controller respectively weights the number of instructions being processed for each thread by the operation cycle count associated with each instruction to generate weighted instruction counts for each thread that represent the processing time of the processing pipe line of the SMT processor occupied by each thread. (Emphasis added.)

As can be seen above, paragraph [0024] clearly discloses that cycle counts refer to the number of counts for processing decoded instructions. Contrary to the Examiner's opinion, Applicants are not reading "cycle counts" too narrowly or too broadly, but rather giving "cycle counts" its ordinary meaning as understood by a person of ordinary skill and as defined in paragraph [0024]. Therefore, the constants C_n of Emer et al. cannot read on the "cycle counts" recited in independent claims 1 and 13.

For at least the reasons given above, claims 1 and 13 are patentable over Emer et al. Dependent claims 2-12 and 14-21 are also patentable for respectively depending on an allowable base claim.

Conclusion

Accordingly, in view of the above amendments and remarks, an early indication of the allowability of each of claims 1-21 in connection with the present application is earnestly solicited.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact John A. Castellano at the telephone number of the undersigned below.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 08-0750 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

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